AMENDMENTS TO THE CLAIMS

Please cancel claims 5 and 7, and add new claims 21-27, in accordance with the following list of claims:

1-2. (Canceled)

3. (Previously Presented) A semiconductor chip package, comprising:

a first integrated semiconductor chip having a first chip size, having a one side and a reverse side, and having a first electrode for wiring on the one side of the first integrated semiconductor chip;

a second integrated semiconductor chip having a second chip size, having a one side and a reverse side, and having a second electrode for wiring on the one side of the second integrated semiconductor chip, the first integrated semiconductor chip being mounted to the second integrated semiconductor chip with the reverse side of the second integrated semiconductor chip facing the reverse side of the first integrated semiconductor chip;

a nonconductive interposer substrate having opposite first and second surfaces, and having a through-hole extending therethrough from the first surface to the second surface, the through-hole being larger than the second chip size;

an adhesive sheet having opposite first and second surfaces, the adhesive sheet being formed of a sheet-shaped adhesive material provided on the interposer substrate at the first surface of the interposer substrate so as to cover the through-hole, the second surface of the adhesive sheet being exposed through the through-hole from a side of the interposer substrate at the second surface of the interposer substrate,

wherein the reverse side of the second integrated semiconductor chip is fixed to the second surface of the adhesive sheet, and the reverse side of the first integrated semiconductor chip is fixed to the first surface of the adhesive sheet so as to face the reverse side of the second integrated semiconductor chip at a position at which the second integrated semiconductor chip is fixed, whereby the second electrode can be wired to external terminals on the second surface of the interposer substrate.

4-5. (Canceled)

6. (Previously Presented) A semiconductor chip package according to claim 3, wherein the interposer substrate has, a sunken region, which is sunken into the side of the interposer substrate at the second surface of the interposer substrate, and the through-hole is provided through the sunken region.

7. (Canceled)

8. (Currently Amended) A semiconductor chip package, comprising:

a first integrated semiconductor chip having a first chip size, having a one side and a reverse side, and having a first electrode for wiring on the one side of the first integrated semiconductor chip;

a second integrated semiconductor chip having a second chip size, having a one side and a reverse side, and having a second electrode for wiring on the one side of the second integrated semiconductor chip, the first integrated semiconductor chip being mounted to the second integrated semiconductor chip with the reverse side of the second integrated semiconductor chip facing the reverse side of the first integrated semiconductor chip;

a nonconductive interposer substrate having opposite first and second surfaces, and having a through-hole extending therethrough from the first surface to the second surface; and

an adhesive sheet formed of sheet-shaped adhesive material at the first surface of the interposer substrate so as to cover the through-hole, the adhesive sheet being larger than the second chip size and having a hole smaller than the second chip size,

wherein the second integrated semiconductor chip is fixed, at the one side of the second integrated semiconductor chip, to the first surface of the interposer substrate via the adhesive sheet, and

wherein the second electrode for wiring is exposed from the side of the interposer substrate at the second surface of the interposer substrate through the

~~adhesive sheet~~ small hole in the adhesive sheet and the through-hole of the interposer substrate.

9. (Canceled)

10. (Previously Presented) A semiconductor chip package according to claim 3, wherein the interposer substrate is formed of one of nonconductive tape and a glass epoxy material.

11. (Canceled)

12. (Previously Presented) A semiconductor chip package according to claim 8, wherein the interposer substrate is formed of one of a nonconductive tape and a glass epoxy material.

13. (Previously Presented) A semiconductor chip package according to claim 3, wherein both surfaces of the adhesive sheet become viscous when heated.

14. (Previously Presented) A semiconductor chip package according to claim 8, wherein both surfaces of the adhesive sheet become viscous when heated.

15. (Previously Presented) A semiconductor chip package according to claim 8, wherein the interposer substrate has external terminals on its second surface to which the second electrode can be wired, and external terminals on its first surface to which the first electrode can be wired.

16. (Previously Presented) A semiconductor chip package according to claim 15, further comprising:

a plurality of solder balls mounted to the second surface of the interposer substrate, the solder balls being electrically connected to respective ones of the external terminals on the first and second surfaces of the interposer substrate.

17-18. (Canceled)

19. (Previously Presented) A semiconductor chip package according to claim 3, wherein the interposer substrate has external terminals on its first surface to which the first electrode can be wired, and the semiconductor chip package further comprises a plurality of solder balls mounted to the second surface of the interposer substrate, the solder balls being electrically connected to respective ones of the external terminals on the first and second surfaces of the interposer substrate.

20. (Canceled)

21. (New) A semiconductor chip package, comprising:

a first integrated semiconductor chip having a first chip size, having a one side and a reverse side, and having a first electrode for wiring on the one side of the first integrated semiconductor chip;

a second integrated semiconductor chip having a second chip size, having a one side and a reverse side, and having a second electrode for wiring on the one side of the second integrated semiconductor chip, the first integrated semiconductor chip being mounted to the second integrated semiconductor chip with the reverse side of the second integrated semiconductor chip facing the reverse side of the first integrated semiconductor chip;

a nonconductive interposer substrate having opposite first and second surfaces, and having a through-hole extending therethrough from the first surface to the second surface; and

an adhesive sheet formed of sheet-shaped adhesive material at the first surface of the interposer substrate so as to cover the through-hole, the adhesive sheet being larger than the second chip size and further having a hole smaller than the second chip size in width and larger than the second chip size in length,

wherein the second integrated semiconductor chip is fixed, at the one side of the second integrated semiconductor chip, to the first surface of the interposer substrate via the adhesive sheet, and

wherein the second electrode for wiring is exposed from the side of the interposer substrate at the second surface of the interposer substrate through the hole in the adhesive sheet and the through-hole of the interposer substrate.

22. (New) A semiconductor chip package according to claim 21, wherein the first chip size is the same as the second chip size.

23. (New) A semiconductor chip package according to claim 8, wherein the first chip size is the same as the second chip size.

24. (New) A semiconductor chip package according to claim 6, wherein the first chip size is the same as the second chip size.

25. (New) A semiconductor chip package according to claim 6, wherein the first chip size is larger than the second chip size.

26. (New) A semiconductor chip package according to claim 3, wherein the first chip size is the same as the second chip size.

27. (New) A semiconductor chip package according to claim 3, wherein the first chip size is larger than the second chip size.